

**Multi-source Agreement (MSA) of  
40 Gbit/s Serial Miniature Device (XLMD2)**

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**XLMD2-05**

**Electrical, Optical and Physical Interfaces of  
ROSA (PIN)**

**Rev. 1.0  
March 13, 2013**

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**Description**

This technical document has been created by the XLMD2 MSA committee. This document is offered to both users and suppliers of 40Gbit/s serial miniature optical device as a basis for a technical agreement. However, it is not a warranted document. Each optical device supplier will have its own datasheet. If the user wishes to find a warranted document, they should consult the datasheet of the chosen optical device supplier.

The MSA committee reserves the rights at any time to add, amend or withdraw technical data contained in this document.

### Revision History

Revision	Date	Purpose/Changes
1.0	March 13, 2013	First public issue

## 1 Scope

The XLMD2 MSA committee has created this technical document to specify the electrical, optical and physical interfaces of optical receiver device. The specifications were based on the investigation of PIN PD ROSA with TIA.

## 2 Reference Documents

**[1] IEC 61754-20**

“Fibre optic connector interfaces – Part 20: Type LC connector family”

**[2] IEC62007-1**

“Semiconductor optoelectronic devices for fibre optic system applications - Part 1: Essential ratings and characteristics”

**[3] IEC62007-2**

“Semiconductor optoelectronic devices for fibre optic system applications - Part 2: Measuring methods”

**[4] IEEE 802.3bg**

“IEEE Standard for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications – Physical Layer and Management Parameters for Serial 40 Gb/s Ethernet Operation Over Single-Mode Fiber”

**[5] ITU-T G. 693**

“Optical interfaces for intra-office systems”

**[6] ITU-T G.709**

“Network node interface for the Optical Transport Network (OTN)”

**[7] ITU-T G,959.1**

“Optical transport networks physical layer interfaces”

**[8] Telcordia GR-253-CORE**

“SONET Transport Systems: Common Generic Criteria”

**[9] Telcordia GR-468-CORE**

“Generic Reliability Assurance Requirements for Optoelectronic Devices Used In Telecommunications Equipment”

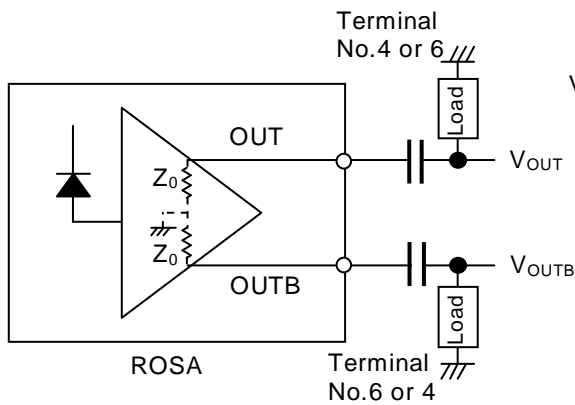
### 3 Abbreviations

<b>CFP</b>	Centum gigabit form-factor pluggable
<b>FPC</b>	Flexible printed circuit
<b>PCB</b>	Printed circuit board
<b>PD</b>	Photo diode
<b>QSFP+</b>	Quad SFP+
<b>ROSA</b>	Receiver optical sub-assembly
<b>SFP+</b>	Enhanced small form-factor pluggable
<b>TIA</b>	Trans-impedance amplifier
<b>TOSA</b>	Transmitter optical sub-assembly

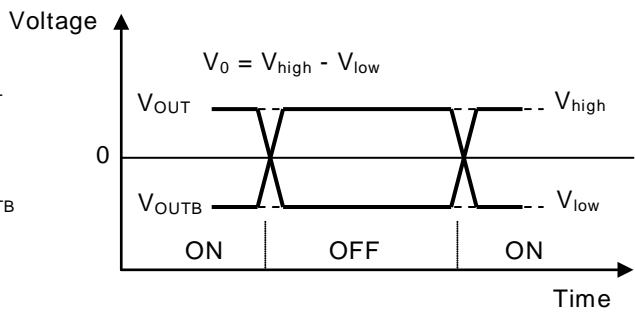
### 4 Electrical Interface

**Table 1 Specifications of electrical and optical performances**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
O/E Conversion gain	G	Single-ended	100	—	—	V/W	
Output impedance	$Z_0$	Single-ended	—	50	—	$\Omega$	Fig. 1
Output voltage swing	$V_0$	Single-ended AC	—	—	0.8	Vpp	Fig. 1 Fig. 2
Power supply voltage	Vpd	—	—	—	5.25	V	PD bias
	Vcc		3.135	3.3	3.465	V	TIA
Power supply current	Icc	—	—	—	150	mA	TIA



**Fig. 1 Definition of the output impedance**



**Fig. 2 Definition of single-ended output**

ON: Optical input on  
 OFF: Optical input off

## 5 Optical Interface

The applicable optical interface shall be specified by each vendor considering the following.

Ethernet (IEEE802.3)	40GBASE-FR
Optical Device	-

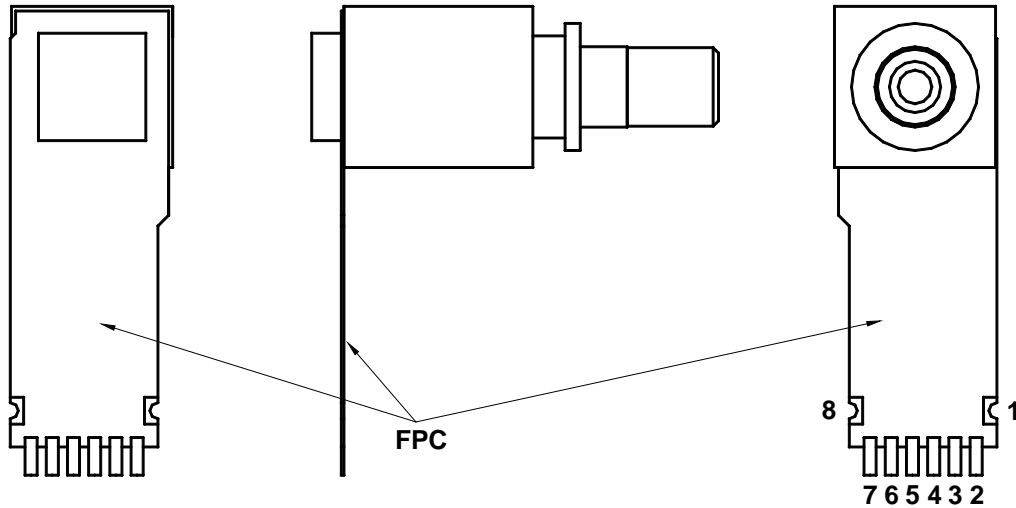
ITU-T (G.693)	VSR2000-3R1	VSR2000-3R2	VSR2000-3R3	VSR2000-3R5
Optical Device	SLM	SLM	SLM	SLM
	VSR2000-3R1F	VSR2000-3R2F	VSR2000-3R3F	VSR2000-3R5F
	SLM	SLM	SLM	SLM
	VSR2000-3L1F	VSR2000-3L2F	VSR2000-3L3F	VSR2000-3L5F
	SLM	SLM	SLM	SLM
	VSR2000-3M1	VSR2000-3M2	VSR2000-3M3	VSR2000-3M5
	SLM	SLM	SLM	SLM
		VSR2000-3H2	VSR2000-3H3	VSR2000-3H5
		SLM	SLM	SLM

ITU-T(G.959)	P1I1-3D1		P1I1-3D3	P1I1-3D5
Source Type	SLM		SLM	SLM
	1S1-3D1F	P1S1-3C2	P1S1-3C3	P1S1-3C5
	SLM	SLM	SLM	SLM
	P1S1-3D1			
	SLM			
	1S1-3D1F			
	SLM			
	P1L1-3C1	P1L1-3A2	P1L1-3A3	P1L1-3A5
	SLM	SLM	SLM	SLM
	1L1-3C1F	1L1-3C2FD	1L1-3C3FD	1L1-3C5FD
	SLM	SLM	SLM	SLM
		1L1-3C2F	1L1-3CF3	1L1-3C5F
		SLM	SLM	SLM

Telcordia (GR-253-CORE)	SR-1		
Optical Device	Indirect Modulation(IM)		
	SR-2	IR-2	IR-3
	IM	IM	IM
		LR-2	LR-3
		IM	IM

## 6 Electrical Interface

### 6.1 Numbering of electrical terminals



**Fig. 3 Electrical terminal numbering assignments**

**Note 1:** The FPC structure in Fig. 3 is prepared as an example only. The vendor should specify its FPC structure based on the mechanical interface in Section 7. The electrical terminal numbering assignments shall be defined by the pattern layout in Fig. 5

### 6.2 Electrical terminal assignment

**Table 2 Terminal function definitions**

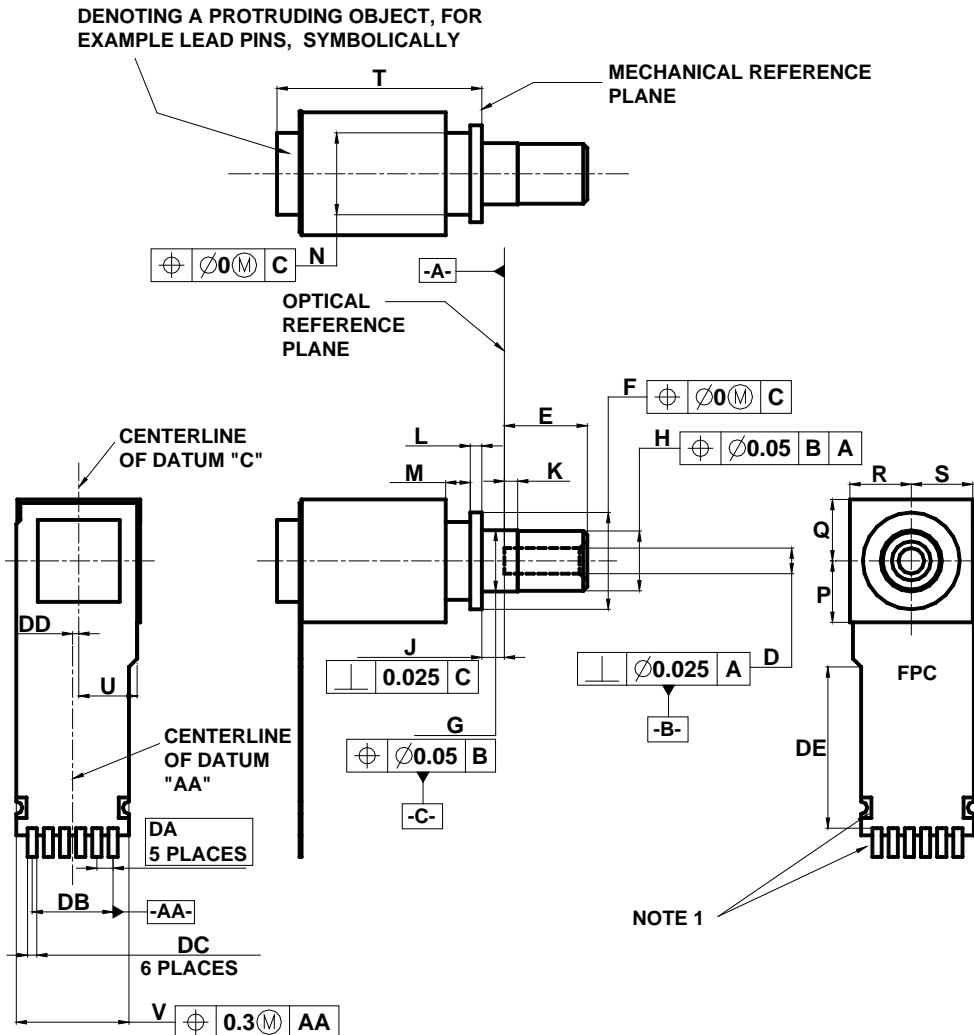
Terminal number	Symbol	Function
1	OP	Option(Input)
2	Vcc	TIA Power Supply
3	GND	Signal Ground
4	OUT/OUTB	Out/OutB
5	GND	Signal Ground
6	OUTB/OUT	OutB/Out
7	GND	Signal Ground
8	PDC	PD Cathode

**Note 1:** Package potential shall be specified by each vendor.

**Note 2:** Definitions of “OUT” and “OUTB can be obtained in Fig. 2.

**7 Mechanical interface**

**7.1 Package outline**



**Fig. 4 Package outline drawing**

**Note 1:** The attachment structure of the FPC to the ROSA body shall be specified by each vendor to comply with the recommended pattern layout described in Fig. 5. The structure described here is prepared as an example only.

**Note 2:** Denoting 8 soldering pads corresponding to the terminals described in Fig. 3 and Table 2. Features and dimensions of the pads and the FPC end portion shape around the pads shall be specified by each vendor to comply with the recommended pattern layout described in Fig. 5. The features of the pads and the FPC end portion shape described in Fig. 4 are prepared as examples only.

**Note 3:** The vendor should design the FPC by considering electrical crosstalk and mechanical stress.



**Table 3 Dimensions of the package outline**

Reference	Dimensions mm		Notes
	Minimum	Maximum	
D	-	-	Note 1
E	4.0	4.1	
F	4.7	5.1	Diameter
G	2.98	3.00	Diameter
H	-	2.97	Diameter
J	1.065	1.135	
K	0.55	0.70	
L	0.52	0.63	
M	1.0	-	
N	-	4.1	Diameter
P	-	3.0	Note 2
Q	-	3.0	Note 2
R	-	3.0	Note 2
S	-	3.0	Note 2
T	-	13.0	Note 3
U	-	3.0	Note 4, Note 5
V	-	5.7	Note 5
DA	0.79		Basic dimension, Note 5
DB	3.95		Reference dimension, Note 5
DC	-	-	Note 6
DD	0.05	0.55	Note 5, Note 7
DE	2.5	-	Note 5

**Note 1:** Refer IEC 61754-20.

**Note 2:** P, Q, R and S only define the maximum dimension, thus do not specify the shape of the package.

**Note 3:** The dimension T shall be specified by each vendor considering their designed FPC attachment structure and the recommended pattern layout described in Fig. 5.

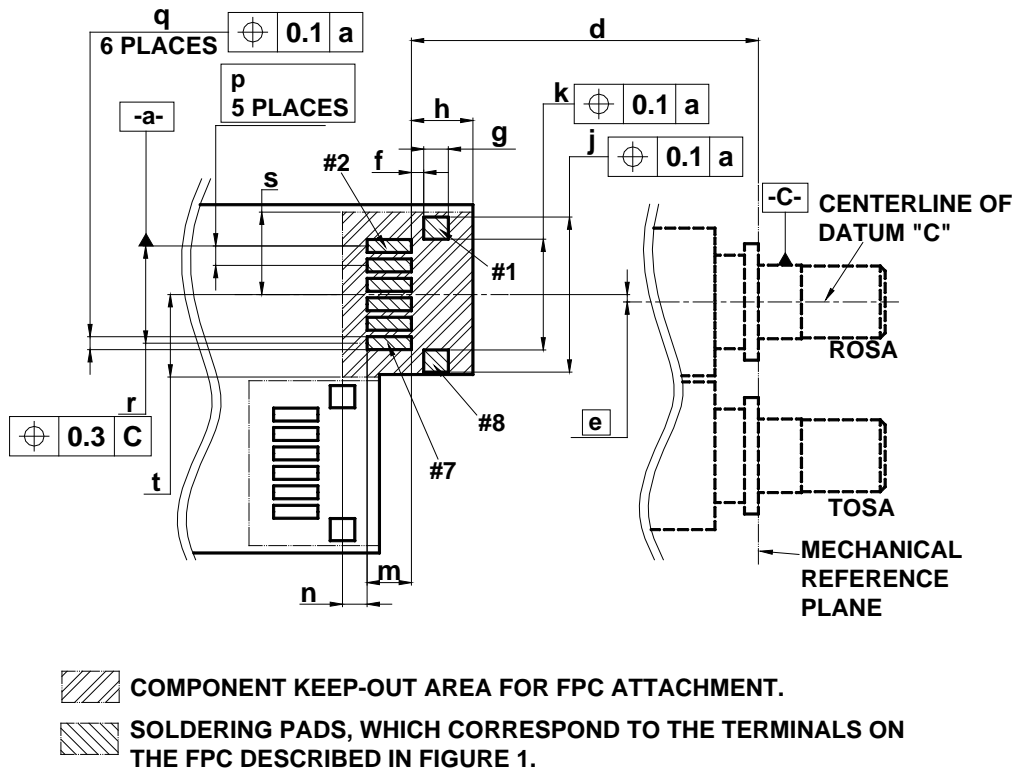
**Note 4:** Denoting the outline dimension of the FPC from the datum "C".

**Note 5:** The dimensions defined in this table shall be satisfied, even if a vendor should choose the different FPC attachment structure or the different FPC end portion shape from those described in Fig. 4.

**Note 6:** The dimension and the positional tolerance of "DC" shall be specified by each vendor considering the recommended pattern layout described in Fig. 5.

**Note 7:** Denoting the dimension from the centerline of the datum “C” to the centerline of the datum “AA”.

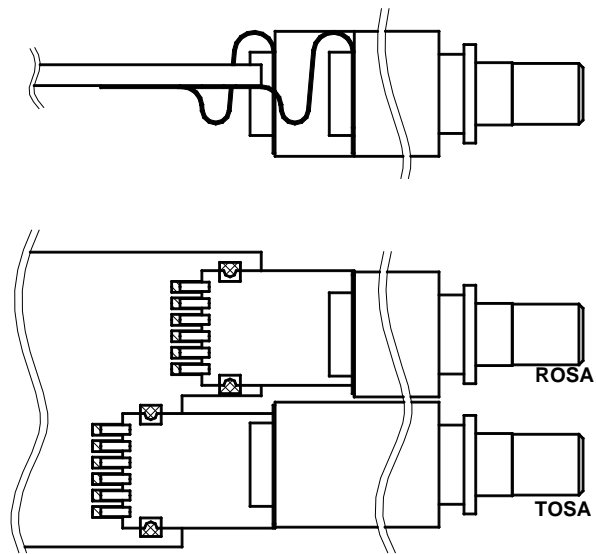
**7.2 Recommended pattern layout**



**Fig. 5 Recommended pattern layout for the PCB in a CFP or QSFP+ package transceiver**

**Note 1:** The datum “C” described here is the same one as described in Fig. 4.

**Note 2:** #1, #2, #7 and #8 in this figure are denoting the pad numbers corresponding to the terminal numbers described in Fig. 3 and Table 2.



**Fig. 6 Recommended arrangement of the PCB, FPCs, TOSA and ROSA**

**Note 1:** The soldering pads for FPC attachment shall be prepared on the top side of the PCB as described here. The bending shape of the FPC shall be specified by each vendor. The FPC bending shape described here is prepared as an example only.

**Table 4 Dimensions of the recommended pattern layout for the PCB**

Reference	Dimensions mm		Notes
	Minimum	Maximum	
d	17.7	18.4	
e	0.3		Basic dimension, Note 1
f	0.50	0.55	
g	1.0	1.1	
h	-	2.5	
j	6.10	6.35	
k	4.45	4.55	
m	1.0	-	
n	1.0	-	
p	0.79		Basic dimension
q	0.45	0.50	
r	3.95		Reference dimension
s	3.35	-	Note 2
t	3.35	-	Note 2

**Note 1:** Denoting the offset between the datum “C” and the datum “a”.

**Note 2:** Denoting the dimension from the datum “a”.