Multi-source Agreement (MSA) of
40 Gbit/s Serial Miniature Device (XLMD2)

XLMD2-04

Electrical, Optical and Physical Interfaces of TOSA (Uncooled DML)

Rev. 1.0
March 13, 2013

Description

This technical document has been created by the XLMD2 MSA committee. This document is offered to both users and suppliers of 40Gbit/s serial miniature optical device as a basis for a technical agreement. However, it is not a warranted document. Each optical device supplier will have its own datasheet. If the users wish to find a warranted document, they should consult the datasheet of the chosen optical device supplier.

The MSA committee reserves the rights at any time to add, amend or withdraw technical data contained in this document.

Revision History

Revision	Date	Purpose / Changes
1.0	March 13, 2013	First public release

1 Scope

The XLMD2 MSA committee has created this technical document to specify the electrical, optical and physical interfaces of optical transmitter devices. The specifications were based on the investigation of TOSA (Uncooled DML).

2 Reference Documents

[1] FDA CDRH21CFR 1040.10
"Performance standards for light-emitting products (Laser products.)"

[2] FDA CDRH21CFR 1040.11
"Performance standards for light-emitting products (Specific purpose laser products.)"

[3] IEC 60825-1
"Safety of laser products-Part 1: Equipment classification, requirements and user's guide"

[4] IEC 60825-2
"Safety of laser products-Part 2: Safety of optical fibre communication systems - Interpretation sheet 1"

[5] IEC 61754-20
"Fibre optic connector interfaces – Part 20: Type LC connector family"

[6] IEC 62007-1
"Semiconductor optoelectronic devices for fibre optic system applications - Part 1: Essential ratings and characteristics"

[7] IEC 62007-2
"Semiconductor optoelectronic devices for fibre optic system applications - Part 2: Measuring methods"

[8] IEEE 802.3bg
"IEEE Standard for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications –Physical Layer and Management Parameters for Serial 40 Gb/s Ethernet Operation Over Single-Mode Fiber"

[9] ITU-T G.693
"Optical interfaces for intra-office systems"

[10] ITU-T G.709
"Network node interface for the Optical Transport Network (OTN)"

[11] ITU-T G.959.1
"Optical transport network physical layer interfaces"

[12] Telcordia GR-253-CORE
"SONET Transport Systems: Common Generic Criteria"

[13] Telcordia GR-468-CORE
"Generic Reliability Assurance Requirements for Optoelectronic Devices Used In Telecommunications Equipment"

3 Abbreviations

CFP Centum gigabit form-factor pluggable
DML Directly modulated laser diode
EMwL External modulator with laser diode
FPC Flexible printed circuit
LD Laser diode
PCB Printed circuit board
PD Photo diode
QSFP+ Quad SFP+
ROSA Receiver optical sub-assembly
SFP+ Enhanced small form-factor pluggable
TEC Thermo-electric cooler
TOSA Transmitter optical sub-assembly

4 Electrical Interface

Table 1 Specifications of electrical and optical performances

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Threshold current	Ith	CW	—	—	50	mA	
Operating current	Iop	CW	—	—	160	mA	
Slope efficiency	η	CW	—	—	—	W/A	Note 1
Operating voltage	Vop	CW	—	—	3.0	V	
Monitor current	Imon	CW	0.05	—	2	mA	
Monitor responsivity		CW	—	—	—	A/W	Note 1
Capacitance (PD)		Vrd=5V	—	—	20	pF	
Dark current (PD)		Vrd=5V	—	—	0.1	μA	
Thermistor resistance	Rth	25degC	9.5	—	10.5	kΩ	
Thermistor B constant	B		3800	3900	4000	K	
Driving LD conditions							
Driver output impedance	Zs		— —	25 50	— —	Ω	Fig. 1

Note 1: Specified by each vendor.

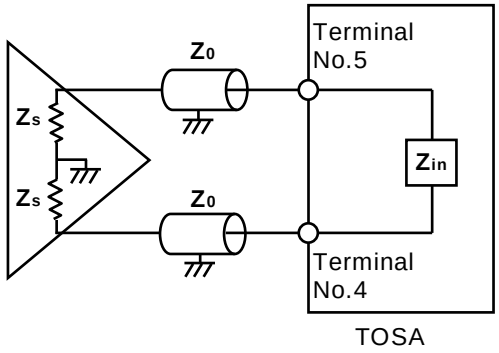

Fig. 1 Definition of the impedances

Z_{in} includes LD, series resistance, etc. Driver output impedance Z_S is only specified in Table 1. The other Z_0 and Z_{in} are specified by each vendor.

5 Optical Interface

The applicable optical interface shall be specified by each vendor. Future standards may be supported.

6 Electrical Interface

6.1 Numbering of electrical terminals

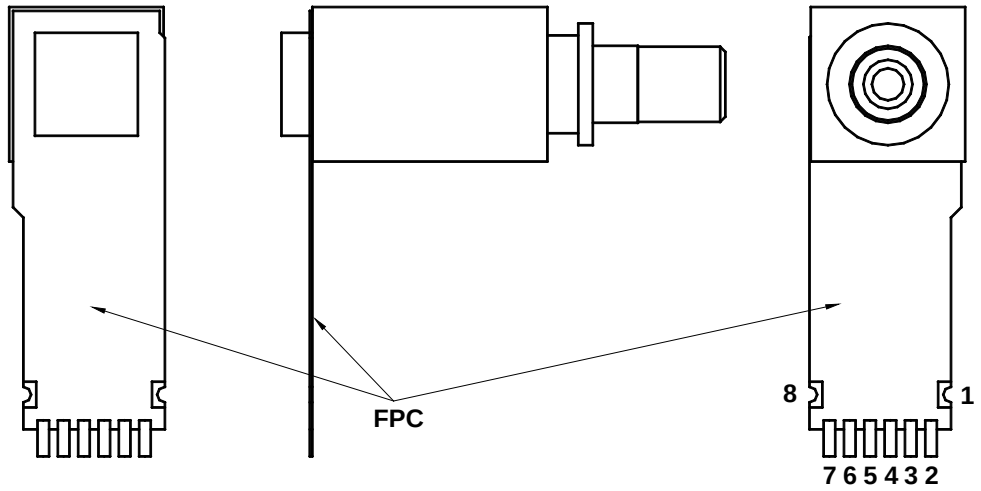

Fig. 2 Electrical terminal numbering assignments

Note 1: The FPC structure in Fig. 2 is prepared as an example only. The vender should specify its FPC structure based on the mechanical interface in Section 7. The electrical terminal numbering assignments shall be defined by the pattern layout in Fig. 4.

6.2 Electrical terminal assignment

Table 2 Terminal function definitions

Terminal number	Symbol	Function (Option 1)	Symbol	Function (Option 2)
1	GND	Signal Ground	GND	Signal Ground
2	PDC	PD Cathode	PDC	PD Cathode
3	GND	Signal Ground	GND	Signal Ground
4	LDC	LD Cathode	LDC	LD Cathode
5	LDA	LD Anode	LDA	LD Anode
6	GND	Signal Ground	GND	Signal Ground
7	TH	Thermistor	NUC	No User Connection
8	GND	Signal Ground	GND	Signal Ground

Note 1: Package potential shall be specified by each vendor.

7 Mechanical interface

7.1 Package outline

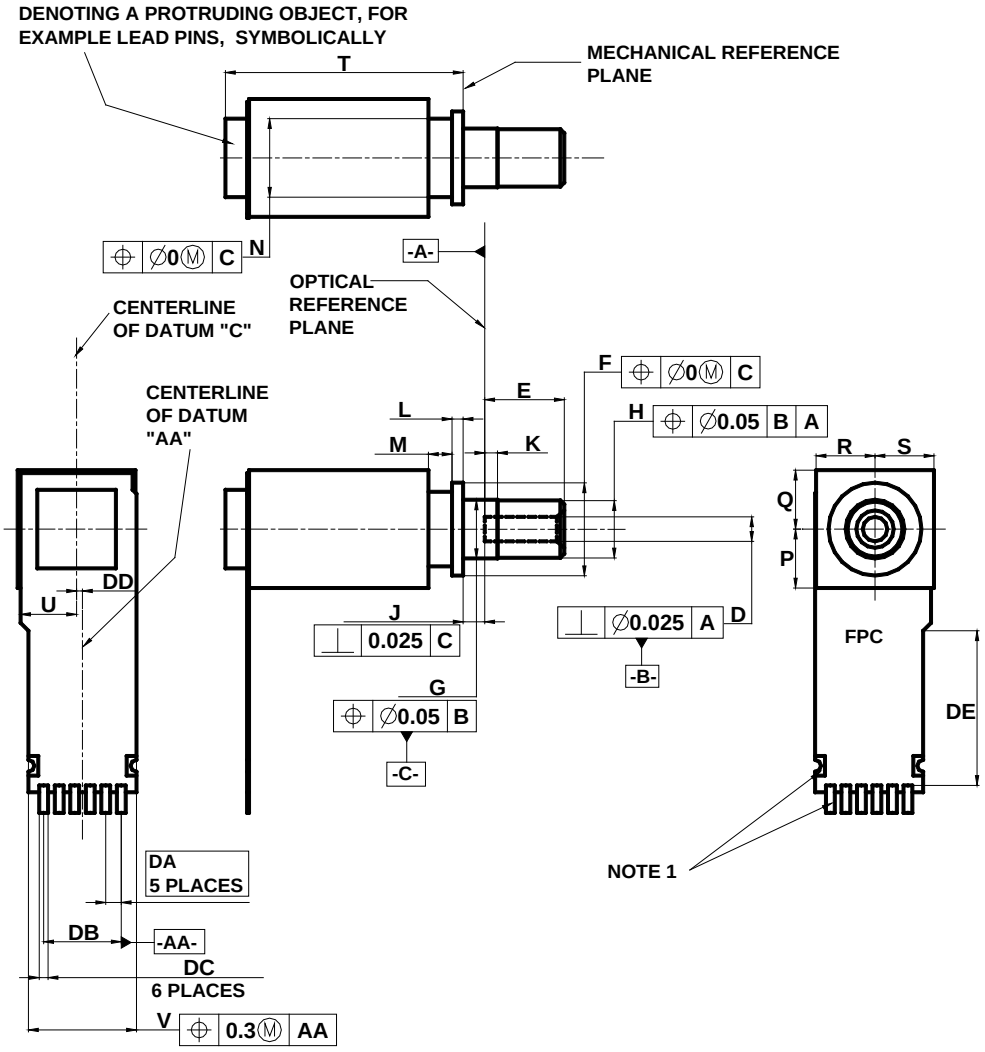

Fig. 3 Package outline drawing

Note 1: The attachment structure of the FPC to the TOSA body shall be specified by each vendor to comply with the recommended pattern layout described in Fig. 4. The structure described here is prepared as an example only.

Note 2: Denoting 8 soldering pads corresponding to the terminals described in Fig. 2 and Table 2. Features and dimensions of the pads and the FPC end portion shape around the pads shall be specified by each vendor to comply with the recommended pattern layout described in Fig. 4. The features of the pads and the FPC end portion shape described in Fig. 3 are prepared as examples only.

Note 3: The vendor should design the FPC by considering electrical crosstalk and mechanical stress.

Table 3 Dimensions of the package outline

Reference	Dimensions mm		Notes
	Minimum	Maximum	
D	-	-	Note 1
E	4.0	4.1	
F	4.7	5.1	Diameter
G	2.98	3.00	Diameter
H	-	2.97	Diameter
J	1.065	1.135	
K	0.55	0.70	
L	0.52	0.63	
M	1.0	-	
N	-	4.1	Diameter
P	-	3.0	Note 2
Q	-	3.0	Note 2
R	-	3.0	Note 2
S	-	3.0	Note 2
T	-	13.8	
U	-	3.0	Note 3, Note 4
V	-	5.7	Note 4
DA	0.79		Basic dimension, Note 4
DB	3.95		Reference dimension, Note 4
DC	-	-	Note 5
DD	0.05	0.55	Note 4, Note 6
DE	2.5	-	Note 4

Note 1: Refer IEC 61754-20.

Note 2: P, Q, R and S only define the maximum dimension, thus do not specify the shape of the package.

Note 3: Denoting the outline dimension of the FPC from the datum “C”.

Note 4: The dimensions defined in Table 3 shall be satisfied, even if a vendor should choose the different FPC attachment structure or the different FPC end portion shape from those described in Fig. 3.

Note 5: The dimension and the positional tolerance of “DC” shall be specified by each vendor considering the pattern layout described in Fig. 4.

Note 6: Denoting the dimension from the centerline of the datum “C” to the centerline of the datum “AA”.

7.2 Recommended pattern layout

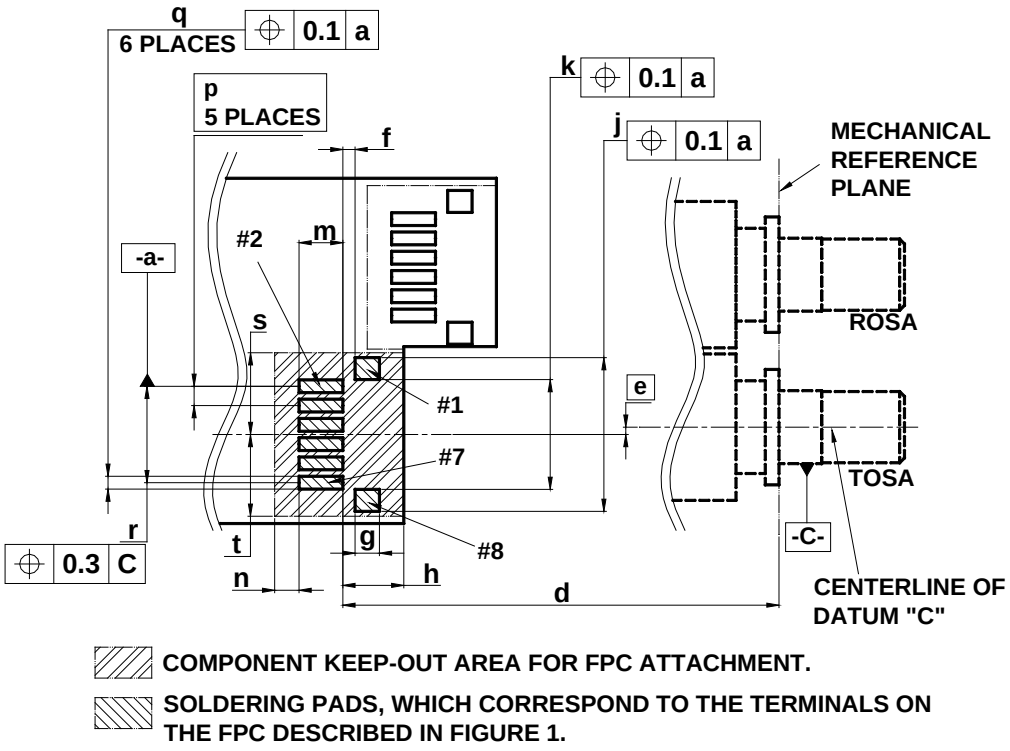

Fig. 4 Recommended pattern layout for the PCB in a CFP or QSFP+ package transceiver

Note 1: The datum “C” described here is the same one as described in Fig. 3.

Note 2: #1, #2, #7 and #8 in Fig.4 are denoting the pad numbers corresponding to the terminal numbers described in Fig. 2 and Table 2.

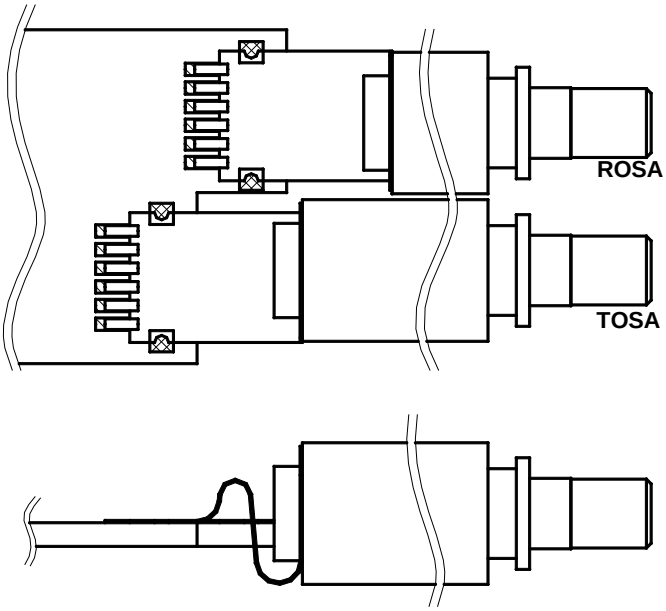

Fig. 5 Recommended arrangement of the PCB, FPCs, TOSA and ROSA

Note 1: The soldering pads for FPC attachment shall be prepared on the top side of the PCB as described here. The bending shape of the FPC shall be specified by each vendor. The FPC bending shape described here is prepared as an example only.

Table 4 Dimensions of the recommended pattern layout for the PCB

Reference	Dimensions mm		Notes
	Minimum	Maximum	
d	18.5	19.2	
e	0.3		Basic dimension, Note 1
f	0.50	0.55	
g	1.0	1.1	
h	-	2.5	
j	6.10	6.35	
k	4.45	4.55	
m	1.0	-	
n	1.0	-	
p	0.79		Basic dimension
q	0.45	0.50	
r	3.95		Reference dimension
s	3.35	-	Note 2
t	3.35	-	Note 2

Note 1: Denoting the offset between the datum “C” and the datum “a”.

Note 2: Denoting the dimension from the datum “a”.