Multi-source Agreement (MSA) of
40 Gbit/s Serial Miniature Device (XLMD2)

XLMD2-02

Electrical, Optical and Physical Interfaces of TOSA (Cooled EMwL)

Rev. 1.0
March 13, 2013

Description

This technical document has been created by the XLMD2 MSA committee. This document is offered to both users and suppliers of 40Gbit/s serial miniature optical device as a basis for a technical agreement. However, it is not warranted document. Each optical device supplier will have its own datasheet. If the user wishes to find a warranted document they should consult the datasheet of the chosen optical device supplier.

The MSA committee reserves the rights at any time to add, amend or withdraw technical data contained in this document

Revision History

Revision	Date	Purpose/ changes
1.0	March 13, 2013	First public issue

1 Scope

The XLMD2 MSA committee has created this technical document to specify the electrical, optical and pysical interfaces of optical transmitter device. The specifications were based on the investigationof TOSA (Cooled EMwL) driven by external driver.

2 Reference Documents

[1] FDA CDRH21CFR 1040.10
"Performance standards for light-emitting products (Laser products.)"

[2] FDA CDRH21CFR 1040.11
"Performance standards for light-emitting products (Specific purpose laser products.)"

[3] IEC 60825-1
"Safety of laser products-Part 1: Equipment classification, requirements and user's guide"

[4] IEC 60825-2
"Safety of laser products-Part 2: Safety of optical fibre communication systems - Interpretation sheet 1"

[5] IEC 61754-20
"Fibre optic connector interfaces – Part 20: Type LC connector family"

[6] IEC62007-1
"Semiconductor optoelectronic devices for fibre optic system applications - Part 1: Essential ratings and characteristics"

[7] IEC62007-2
"Semiconductor optoelectronic devices for fibre optic system applications - Part 2: Measuring methods"

[8] IEEE 802.3bg
"IEEE Standard for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications –Physical Layer and Management Parameters for Serial 40 Gb/s Ethernet Operation Over Single-Mode Fiber"

[9] ITU-T G.693
"Optical interfaces for intra-office systems"

[10] ITU-T G709
"Network node interface for the Optical Transport Network (OTN)"

[11] ITU-T G.959.1
"Optical transport network physical layer interfaces"

[12] Telcordia GR-253-CORE
"SONET Transport Systems: Common Generic Criteria"

[13] Telcordia GR-468-CORE
"Generic Reliability Assurance Requirements for Optoelectronic Devices Used In Telecommunications Equipment"

3 Abbreviations

CFP	Centum gigabit form-factor pluggable
DML	Directly modulated laser diode
EMwL	External modulator with laser diode
FPC	Flexible printed circuit
LD	Laser diode
PCB	Printed circuit board
PD	Photo diode
QSFP+	Quad SFP+
ROSA	Receiver optical sub-assembly
SFP+	Enhanced small form-factor pluggable
TEC	Thermo-electric cooler
TOSA	Transmitter optical sub-assembly

4 Electrical Interface

Table 1 Specifications of electrical and optical performances

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Threshold current	Ith	CW	—	—	50	mA	
LD operating current	Iop				200	mA	
LD operating voltage	Vop	CW	—	—	3.0	V	
On-level modulation voltage	Vo		-1.0	—	0	V	Fig. 1
Modulator drive voltage	Vpp		—	—	2.3	V	Fig. 1
Input impedance	Zin		—	50	—	Ω	Fig. 2
Monitor current	Imon	CW	0.05	—	2	mA	
Capacitance (PD)		Vrd = 5 V	—	—	20	pF	
Dark current (PD)		Vrd = 5 V	—	—	0.1	μA	
TEC current	Itec		—	—	1	A	
TEC voltage	Vtec		—	—	2	V	
TEC power consumption	Ptec		—	—	1.3	W	
Thermistor resistance	Rth	25degC	9.5	—	10.5	kΩ	
Thermistor B constant	B		3800	3900	4000	K	

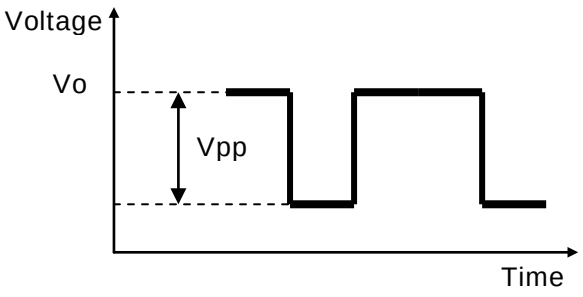

Fig.1 Definition of modulation voltage

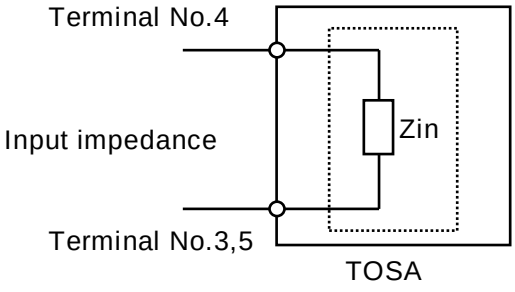

Fig.2 Definition of input impedance

5 Optical Interface

The applicable optical interface shall be specified by each vendor considering the following.

Ethernet (IEEE802.3bg)	40GBASE-FR
Optical Device	-

ITU-T (G.693)	VSR2000-3R1	VSR2000-3R2	VSR2000-3R3	VSR200-3R5
Optical Device	SLM	SLM	SLM	SLM
	VSR2000-3R1F	VSR2000-3R2F	VSR2000-3R3F	VSR2000-3R5F
	SLM	SLM	SLM	SLM
	VSR2000-3L1F	VSR2000-3L2F	VSR2000-3L3F	VSR2000-3L5F
	SLM	SLM	SLM	SLM
	VSR2000-3M1	VSR2000-3M2	VSR2000-3M3	VSR2000-3M5
	SLM	SLM	SLM	SLM
		VSR2000-3H2	VSR2000-3H3	VSR2000-3H5
		SLM	SLM	SLM

ITU-T (G.959)	P1I1-3D1		P1I1-3D3	P1I1-3D5
Source Type	SLM		SLM	SLM
	1S1-3D1F	P1S1-3C2	P1S1-3C3	P1S1-3C5
	SLM	SLM	SLM	SLM
	P1S1-3D1			
	SLM			
	1S1-3D1F			
	SLM			
	P1L1-3C1	P1L1-3A2	P1L1-3A3	P1L1-3A5
	SLM	SLM	SLM	SLM
	1L1-3C1F	1L1-3C2FD	1L1-3C3FD	1L1-3C5FD
	SLM	SLM	SLM	SLM
		1L1-3C2F	1L1-3C3F	1L1-3C5F
		SLM	SLM	SLM

Telcordia (GR253-CORE)	SR-1		
Optical Device	Indirect Modulation (IM)		
	SR-2	IR-2	IR-3
	IM	IM	IM
		LR-2	LR-3
		IM	IM

6 Electrical Interface

6.1 Numbering of electrical terminals

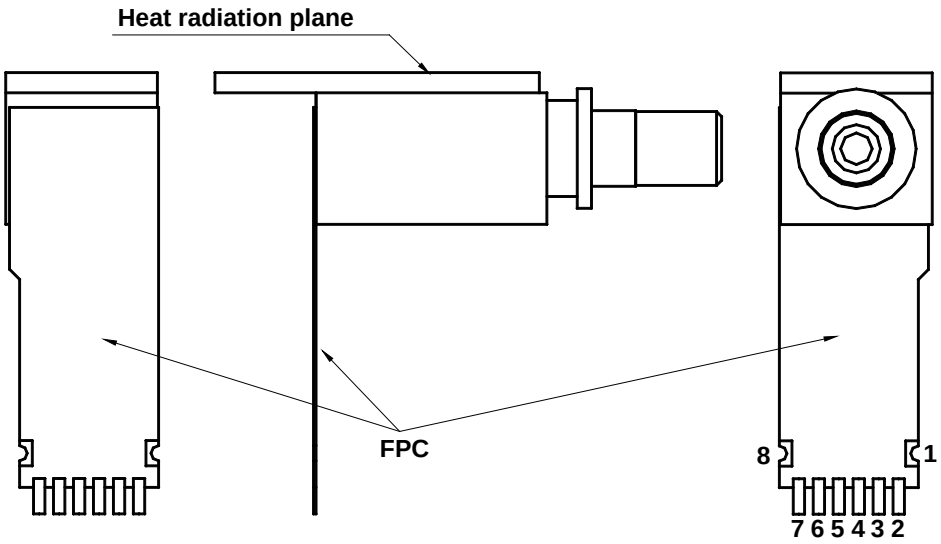

Fig. 3 Electrical terminal numbering assignments

Note 1: The FPC structure in Fig.3 is prepared as an example only. The vender should specify its FPC structure based on the mechanical interface in Section 7. The electrical terminal numbering assignments shall be defined by the pattern layout in Fig. 5.

6.2 Electrical terminal assignment

Table 2 Terminal function definitions

Terminal number	Symbol	Function
1	TEC (-)	TEC Cathode
2	TEC (+)	TEC Anode
3	GND	Signal Ground
4	IN	Modulator Anode
5	GND	Signal Ground
6	PDA	PD Anode
7	LDA	LD Anode
8	TH	Thermistor

Note 1: Package potential shall be specified by each vendor.

Note 2: TEC acts as an LD-chip-cooler in the bias direction described here. When it is biased reversely, its function is changed into heating.

7 Mechanical interface

7.1 Package outline

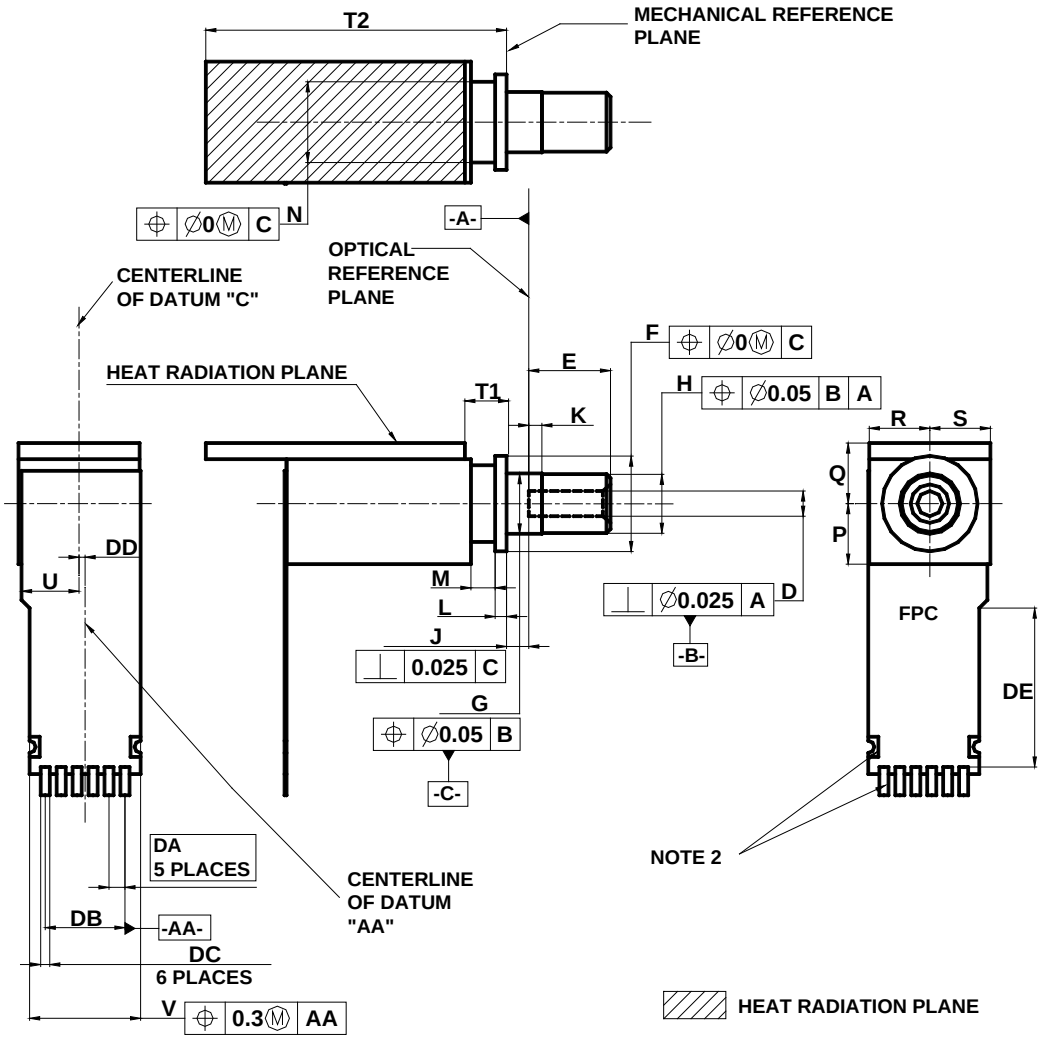

Fig. 4 Package outline drawing

Note 1: The attachment structure of the FPC to the TOSA body shall be specified by each vendor to comply with the recommended pattern layout described in Fig. 5. The structure described here is prepared as an example only.

Note 2: Denoting 8 soldering pads corresponding to the terminals described in Fig. 3 and Table 3. Features and dimensions of the pads and the FPC end portion shape around the pads shall be specified by each vendor to comply with the recommended pattern layout described in Fig. 5. The features of the pads and the FPC end portion shape described in this figure are prepared as examples only.

Note 3: The vendor should design the FPC by considering electrical crosstalk and mechanical stress.

Table 3 Dimensions of the package outline

Reference	Dimensions Mm		Notes
	Minimum	Maximum	
D	-	-	Note 1
E	4.0	4.1	
F	4.7	5.1	Diameter
G	2.98	3.00	Diameter
H	-	2.97	Diameter
J	1.065	1.135	
K	0.55	0.70	
L	0.52	0.63	
M	1.0	-	
N	-	4.1	Diameter
P	-	3.0	Note 2
Q	2.6	3.0	Note 2
R	-	3.0	Note 2
S	-	3.0	Note 2
T1	1.52	-	
T2	-	13.8	
U	-	3.0	Note 3, Note 4
V	-	5.7	Note 4
DA	0.79		Basic dimension, Note 4
DB	3.95		Reference dimension, Note 4
DC	-	-	Note 5
DD	0.05	0.55	Note 4, Note 6
DE	2.5	-	Note 4

Note 1: Refer IEC 61754-20.

Note 2: Denoting the outline dimension of the TOSA body, including the heat radiation plane, from the datum “C”.

Note 3: Denoting the outline dimension of the FPC from the datum “C”.

Note 4: The dimensions defined in Table 3 shall be satisfied, even if a vendor should choose the different FPC attachment structure or the different FPC end portion shape from those described in Fig. 4.

Note 5: The dimension and the positional tolerance of “DC” shall be specified by each vendor considering the recommended pattern layout described in Fig. 5.

Note 6: Denoting the dimension from the centerline of the datum “C” to the centerline of the datum “AA”.

7.2 Recommended pattern layout

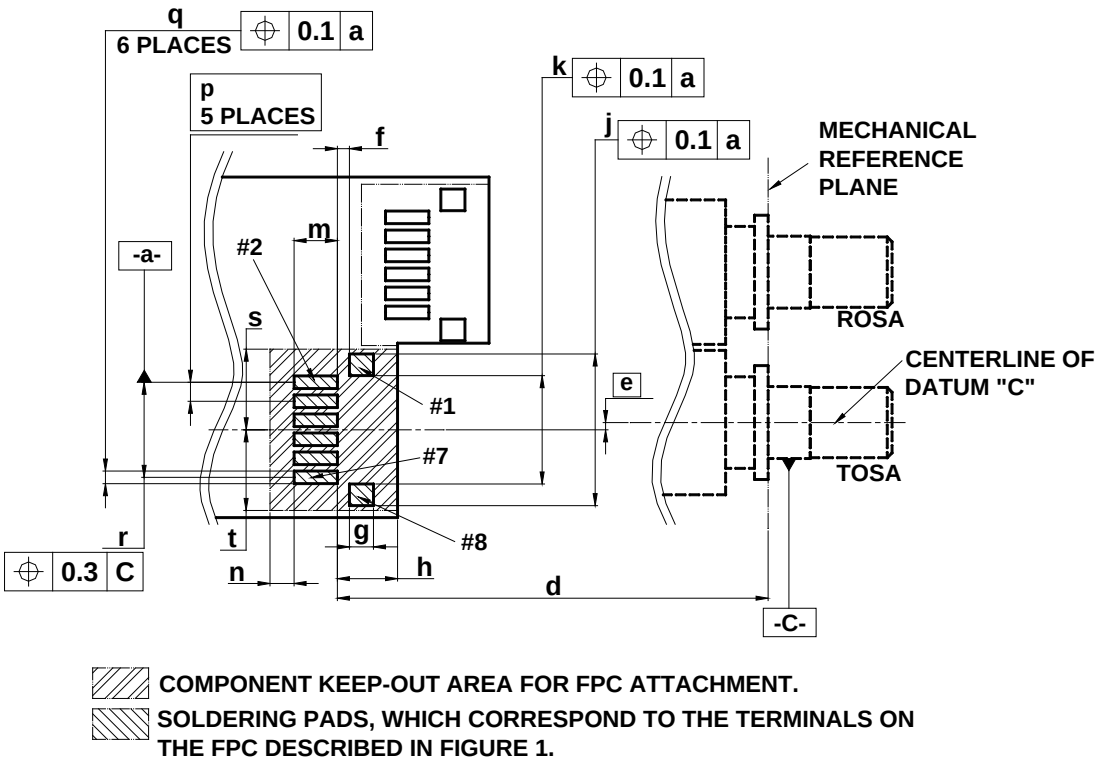

Fig. 5 Recommended pattern layout for the PCB in a CFP or QSFP+ package transceiver

Note 1: The datum “C” described here is the same one as described in Fig. 4.

Note 2: #1, #2, #7 and #8 in Fig. 5 are denoting the pad numbers corresponding to the terminal numbers described in Fig. 3 and Table 2.

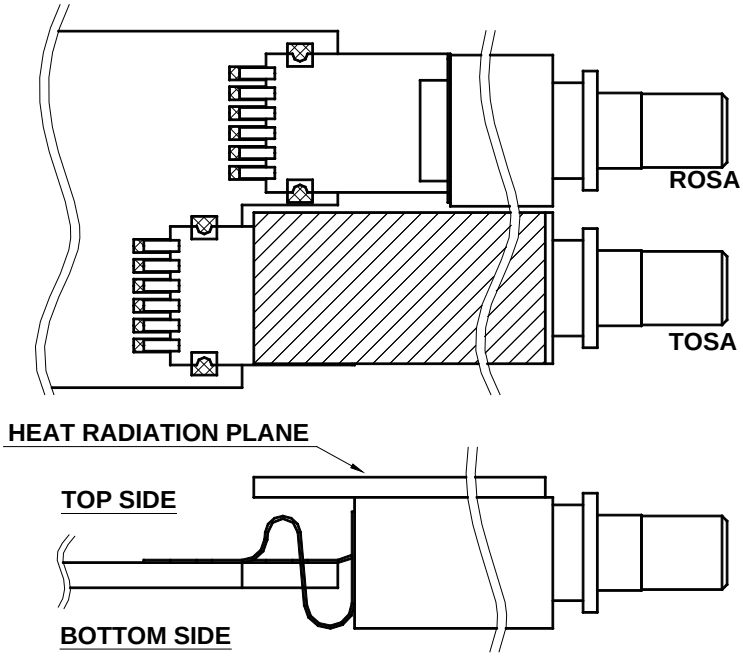

Fig. 6 Recommended arrangement of the PCB, FPCs, TOSA and ROSA

Note 1: The soldering pads for FPC attachment shall be prepared on the top side of the PCB as described here. The bending shape of the FPC shall be specified by each vendor. The FPC bending shape described here is prepared as an example only.

Table 4 Dimensions of the recommended pattern layout for the PCB

Reference	Dimensions mm		Notes
	Minimum	Maximum	
d	18.5	19.2	
e	0.3		Basic dimension, Note 1
f	0.50	0.55	
g	1.0	1.1	
h	-	2.5	
j	6.10	6.35	
k	4.45	4.55	
m	1.0	-	
n	1.0	-	
p	0.79		Basic dimension
q	0.45	0.50	
r	3.95		Reference dimension
s	3.35	-	Note 2
t	3.35	-	Note 2

Note 1: Denoting the offset between the datum “C” and the datum “a”.

Note 2: Denoting the dimension from the datum “a”.